FIR Equalization using tuned continuous-time delay elements based on Transmission Lines or Lumped Passive Components

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(1) description

Copper and Fiber Optic serial links both may benefit from equalization of received and/or transmitted signals. Due the high speed of operation for such links, digital solutions are often not feasible and equalizer circuits must operate on analog signals that are either discrete time or continuous time.

A common method of equalization is an FIR filter based on sampled (discrete-time) data. In its simplest form, the FIR consist of a chain of analog sample-and-hold circuits that feed analog multipliers, as shown in Figure 1.

One of the drawbacks of sampling is that the absolute sampling phase may not be controllable, as is the case in an open-loop system where the clock/data recovery (CDR) is performed after the equalizer. One common solution to use a fractionally spaced equalizer, meaning that the sampling period is some fraction T/n of the data period T. The fractionally spaced EQ is less sensitive to sampling phase. The fractional method has the drawback of burdening the sampling and computational circuits with a higher frequency of operation. Moreover, a discrete-time output may not be suitable for driving a CDR, because CDR circuits for serial links typicaly are designed to operate on a continuous waveform.

As an alternative, one may use an FIR structure with non-sampling (i.e. continuous time) delay elements, as indicated in Figure 2. The difficulty then arises of ensuring an accurate sample delay of T (or whatever is the desired value) while constructing each delay element from one or more possible passive components: Transmission lines, stubs and lumped or semi-lumped resistances and reactances.

To solve the problem of ensuring accurate delay, one may enclose the delay line in a delay-locked loop where the delay is automatically tuned/calibrated by adjusting some of the components, either via direct delay measurement or in a master/slave fashion based on the measurements of a matching delay structure. Figure 3 shows a possible architecture based on the master/slave matching principle. The adjustment can be of any practical form, for example switching in/out capacitances, resistances, inductances and even pieces of transmission line in any parallel and/or serial fashion. The preferred embodiment consist of transmission line segments loaded with switched capacitances.

The tuned delay line thereafter forms the delay portion of an FIR filter that is continuous in time and which output therefore can be sampled at any time instant by the succeeding CDR circuit.

While removing the need for fractional clocking and improving overall performance, the continous nature of the delay line puts added strain on the bandwidth of the FIR coefficient analog multipliers. The multipliers must be fast enough not to distort the output of the filter. Another design issue is the possibly non-ideal gain and phase response of the delay elements. This can to some extent be alleviated by adjusting the FIR filter coefficients, but it may also be possible to use the tuning elements (passive filters) and/or external/intra-stage active amplifiers to reduce or remove the problem.

In the area of magnetic recording channels, an approach has been

demonstrated that uses continuous-time delay elements constructed from lumped active bipolar all-pass filters [Parsi1996]. However, this approach becomes very difficult to implement at higher speeds, such as 10Gb/s serial links, where the unit delay of T=100ps is very small compared to the group delay of a typical active filter based on CMOS technology. It should also be noted that [Parsi1996] does NOT use a DLL to tune the delay elements.

For more detail on the construction of on-chip and off-chip transmission lines, as well as the preferred design of a DLL to calibrate such transmission lines, please refer to the patent application [Sidiropolous2002]. For the purpose of this patent disclosure, we should add that the delay elements may also be constructed using on-chip or off-chip lumped or semi-lumped resistors, inductors and capacitors in addition to more traditional transmission line elements.

(2) figures

Figure 1: Analog discrete-time FIR equalizer
Figure 2: Analog continuous-time FIR equalizer
Figure 3: Master-slave tuning/calibration of delay line for CT-FIR filter
Figure 4: Transposed form continuous-time FIR equalizer

(3) references

[Parsi1996]: K. Parsi, R. Burns, A. Chaiken, M. Chambers, B. Forni, D. Harnishfeger, S. Kaylor, M. Pennell, J. Perez, N. Rao, M. Rohrbaugh, M. Ross, G. Stuhlmiller, "A PRML Read/Write Channel IC Using Analog Signal Processing for 200 Mb/s HDD," 1996 IEEE Journal of Solid-State Circuits, vol. 31 (No. 11), pp. 1817-1830, Nov. 1996.

[Sidiropolous2002]: S. Sidiropoulos and H.J. Liaw. Method and apparatus for clock and data recovery using transmission lines. Patent Application, May 2002.

3) S/H FIR.

Figures for CT-FIR Disclosure

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Figure 1:
Analog Discrete-Time FIR

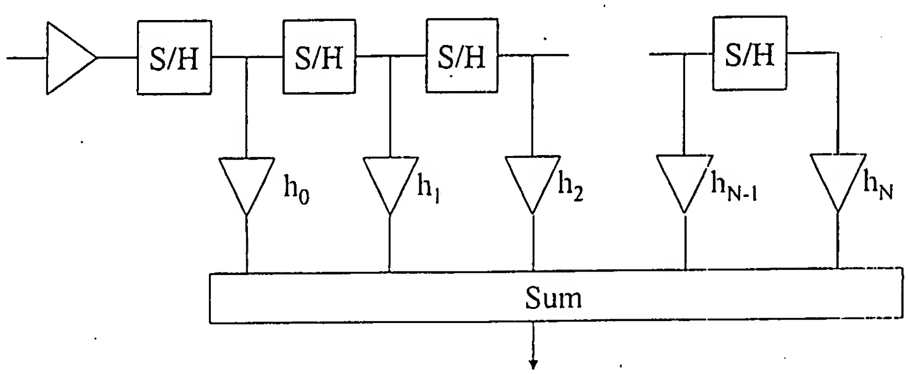

Figure 2:
Analog Continuous-Time FIR

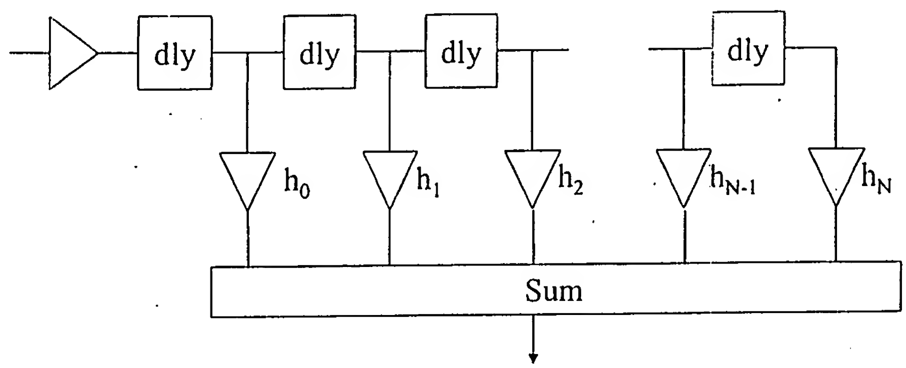

Figure 3:
Master/Slave Tuning